IN THE CLAIMS:

1.-22. (Cancel)

23. (Previously Presented) A method for avoiding effects due to a misalignment that may occur between features in an interconnect structure of a semiconductor device, the interconnect structure having a dielectric material deposited over an underlying interconnect layer and having a via extending through the dielectric material for establishing a connection between an underlying conductor and a trench in an upper portion of the dielectric material, said method comprising the steps of:

(a) forming a mask layer over the dielectric material, said mask layer comprising at least two pairs of mask films;

(b) etching the mask layer to a first predetermined depth forming a via within the mask layer without exposing the underlying dielectric material;

(c) etching the mask layer to a second predetermined depth of the mask layer less than the first predetermined depth forming a trench within the mask layer without exposing the underlying dielectric material;

(d) in the event a misalignment occurs between the via and the trench within said mask layer, removing from the via within said mask layer a material left in said via due to said misalignment, thereby restoring the via within said mask layer to its original size;

(e) forming a via through the dielectric material to the underlying conductor corresponding to the dimensions of the via formed within the mask layer; and

(f) forming a trench in the dielectric material to a predetermined depth of the dielectric material corresponding to the dimensions of the trench formed within the mask layer, thereby ensuring dimensional correspondence of

the via and trench in the dielectric material to the via and trench within the mask layer notwithstanding the occurrence of said misalignment.

24. (Previously Presented) The method of claim 23 wherein a layer of photoresist constitutes the material removed from the via within said mask layer.

25. (Previously Presented) The method of claim 23 wherein the via and trench formed within the mask layer constitute the features in the interconnect structure where said misalignment may occur.

26. (Previously Presented) The method of claim 23 wherein said dielectric material comprises a via dielectric layer formed over the interconnect layer, a barrier layer disposed between the via dielectric layer and the interconnect layer, a trench dielectric layer formed over the via dielectric layer, and an etch stop layer disposed between the trench dielectric layer and the via dielectric layer.

27. (Previously Presented) The method of claim 26 wherein the step of forming the via comprises etching the via through the via dielectric layer and the barrier layer, and the step of forming the trench comprises etching the trench through the trench dielectric layer.

28. (Previously Presented) A method for avoiding effects due to a misalignment that may occur between features in an interconnect structure using a mask layer deposited over a dielectric material which has been deposited over an underlying interconnect layer, said method comprising the steps of:

(a) forming a first mask film over the dielectric material having a known set of etch properties;

(b) forming a second mask film over the first mask film having a known set of etch properties different from the etch properties of the first mask film;

(c) forming a third mask film over the second mask film having etch properties substantially identical to the etch properties of the first film;

(d) forming a fourth mask film over the third mask film having etch properties substantially identical to the etch properties of the second mask film;

(e) etching the second, third and fourth mask films to form a via within the mask layer to a first predetermined depth and down to the first mask film without exposing the underlying dielectric layer;

(f) etching at least the fourth mask film to form a trench within the mask layer to a second predetermined depth less than the first predetermined depth of the mask layer previously etched in the mask layer without exposing the underlying dielectric material; and

(g) in the event a misalignment occurs between the via and the trench within said mask layer, removing from the via within said mask layer a material left in said via due to said misalignment, thereby restoring the via within said mask layer to its original size.

29. (Previously Presented) The method of claim 28 wherein the via and trench formed within the mask layer constitute the features in the interconnect structure where said misalignment may occur.

30. (Currently Amended) The method of claim 28 wherein the interconnect layer includes a conductor and further comprising the steps of forming a via through the dielectric material to the underlying conductor corresponding to the dimensions of the via formed within the mask layer, and forming a trench in the dielectric material to a predetermined depth of the

dielectric material corresponding to the dimensions of the trench formed within the mask layer.

31. (Previously Presented) The method of claim 28 further comprising the steps of etching the first mask film to process the via in the mask layer to expose the underlying dielectric material, and etching the third mask film to form the trench in the mask layer down to the second mask film.

32. (Previously Presented) The method of claim 31 further comprising the steps of forming a via through the dielectric material, and forming a trench in the dielectric material to a predetermined depth of the dielectric material after forming a trench in the mask layer down to the first mask film.

33. (Previously Presented) The method of claim 32 further comprising the step of removing the third and fourth mask films from the semiconductor device.

34. (Previously Presented) The method of claim 32 further comprising the step of removing the second, third, and the fourth mask films from the semiconductor device.

35. (Previously Presented) The method of claim 31 further comprising the steps of forming a via dielectric layer over the underlying interconnect layer, forming a trench dielectric layer over the via dielectric layer, forming an etch stop layer between the via dielectric layer and trench dielectric layer.

36. (Previously Presented) The method of claim 35 further comprising the steps of etching the via in the trench dielectric layer in accordance

with dimensions of the via formed in the mask layer, then simultaneously etching the etch stop layer and the fourth mask film from the semiconductor device.

37. (Currently Amended) The method of claim ~~30~~ 35 further comprising the step of forming a barrier layer between the via dielectric layer and the interconnect layer.

38. (Previously Presented) The method of claim 37 further comprising the steps of etching the via in the via dielectric layer to the barrier layer in accordance with dimensions of the via formed in the mask layer, then simultaneously etching the barrier layer and removing the third mask film from the semiconductor device.

39. (Previously Presented) The method of claim 38 further comprising the steps of forming the trench in the trench dielectric layer, and simultaneously forming the via in the via dielectric layer before etching the barrier layer.

40. (Currently Amended) A semiconductor device having a dielectric material deposited over an underlying interconnect layer, said semiconductor comprising:

a mask layer arranged over the dielectric material for avoiding effects due to a misalignment that may occur between features in an interconnect structure of the semiconductor device, said mask layer comprising:

a first mask film adjacent to the dielectric material and having a known set of etch properties;

a second mask film over the first mask film having a known set of etch properties different from the etch properties of the first mask film;

a third mask film over the second mask film having etch properties substantially identical to the etch properties of the first film; and

a fourth mask film over the third mask film having etch properties substantially identical to the etch properties ~~to the etch properties~~ of the second mask film, wherein at least some of the mask films are etched to a first predetermined depth of the mask layer without exposing the underlying dielectric to form a via within the mask layer, further wherein at least some of the mask films are etched to a second predetermined depth of the mask layer which is less than the depth of the via previously etched in the mask layer to form a trench within the mask layer without exposing the underlying dielectric material; and

a material left in said via due to said misalignment being removable without affecting the underlying dielectric, thereby restoring the via within said mask layer to its original size prior to forming interconnect features in the dielectric material.

41. (Currently Amended) The semiconductor device of claim 40 wherein the interconnect layer includes a conductor and further comprising a via through the dielectric material to the underlying conductor corresponding to the dimensions of the via formed within the mask layer and a trench in the dielectric material to a predetermined depth of the dielectric material corresponding to the dimensions of the trench formed within the mask layer, thereby ensuring dimensional correspondence of the via and trench in the dielectric material to the via and trench within the mask layer notwithstanding the occurrence of said misalignment.